REMARKS

Claims 1-9, 11-18, and 21-34 are pending in the application.

The Examiner rejects claims 15 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regards as their invention.

The Examiner rejects claim 15 under 35 U.S.C. § 102(b) as being anticipated by the acknowledged prior art of Figure 2 ("APA").

The Examiner rejects claims 15, 16, 29, and 30 under 35 U.S.C. § 102(b), as being anticipated by Klein, U.S. Patent No. 6,349,051, ("Klein").

The Examiner rejects claims 1, 4, 5, 12-14, 25, 26, and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of APA.

Applicants amend claim 15.

Claims 1-9, 11-18, and 21-34 remain in the application.

Applicants add no new matter and request reconsideration.

Claims Allowed

The Applicants thank Examiner Dang for the allowance of claims 9, 11, 17, 18, 21-24, and 31.

Claim Rejections – 35 U.S.C. § 112

The Examiner rejects claims 15 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regards as their invention.

Applicants amend claim 15 to obviate the Examiner's rejection. For further clarity Applicants respectfully direct the Examiner to specific portions of specification. See, e.g., paragraphs beginning on page 8, line 23, page 9, line 7, and page 12, line 18, and Figures 4, 5, and 7. For instance, the specification recites, "the memory controller embeds, within its address/command signals, information that *identifies the memory unit*, device, or rank *selected for a particular read or write operation*. For instance, with six ranks, six *unique read commands* (READ*n*, where *n* identifies a rank between 0 and 5, inclusive) are defined," and "[t]he address/command decoder on *each memory device decodes each read* or write *command issued by the memory controller*, regardless of whether chip select has been asserted for that device." See Specification, page 8, line 23 – page 9, line 2, page 9, lines 7-10, and page 12, lines 18-20. Thus, the above-recited references to the specification, when

read in conjunction with their corresponding figures, clearly illustrate that a READ command signal(s) uniquely identifies which memory unit is to perform the read operation, and that the memory unit to perform the operation is identified to all of the memory units. Applicant requests that in view of the above references of the specification and the claim amendment that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 102 and § 103

The Examiner rejects claim 15 under 35 U.S.C. § 102(b) as being anticipated by APA. Applicants respectfully traverse the Examiner's rejection.

Amended claim 15 recites *the READ command signals identify, to each memory unit, which memory unit of the multiple memory units is to perform a data read operation.* The Examiner alleges the APA discloses the recited limitation. APA's command signals, however, "instruct a memory device as to what ***type of operation is to be performed,*** e.g., read, write, refresh," not which memory unit of the multiple memory units is to perform the operation. See Specification, page 1, line 18 – page 2, line 8. Since APA's command signals do not disclose identifying the memory unit currently being addressed, the APA, therefore, does not anticipate claim 15 or its corresponding dependent claim.

The Examiner rejects claims 15, 16, 29, and 30 under 35 U.S.C. § 102(b), as being anticipated by Klein. The Examiner rejects claims 1, 4, 5, 12-14, 25, 26, and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of APA. Applicants respectfully traverse the Examiner's rejection.

Claim 15 recites *an address/command generator to generate address and command signals for multiple memory units, including READ command signals, wherein the READ command signals identify, to each memory unit, which memory unit of the multiple memory units is to perform a data read operation.* Claim 25 recites a similar limitation.

The Examiner alleges Klein's control signals 68 and memory module 60 disclose the recited READ command signals and memory unit, respectively. Klein states control signals 68, such as "row address strobe (RAS)" for signaling each memory module 60 to accept an address signal as a row address, "column address strobe (CAS)" for signaling each memory module 60 to accept an address signal as a column address, and "write enable (WE)" for indicating the type of memory operation to be performed on memory module 60, are "familiar to those in the art." Klein, col. 5, ll. 52-55; col. 6, ll. 4-7. None of these control signals 68, however, disclose identifying which memory module 60 among a plurality of

memory modules 35 is to perform the recited data read operation. See Klein, col. 6, ll. 31-51; Figures 3 and 7. Klein, therefore, does not anticipate claim 15, or claim 25, and their corresponding dependent claims.

Claim 12 recites *a controllable line termination circuit to terminate signals at the data port.* Claims 1, 25, and 29 recite a similar limitation.

The Examiner alleges Klein's transfer gates 64 disclose the recited data bus line termination circuit. However, "[c]laims are not to be read in a vacuum and while it is true they are to be given the broadest *reasonable* interpretation during prosecution, their terms still have to be given the meaning called for by the specification of which they form a part." *In re Royka*, 180 USPQ 580, 582-83 (CCPA 1974). Therefore, when enabled, a *termination circuit* must absorb signals propagating down a data line stub, thus diminishing the amount of energy reflected on the stub. Specification, page 2, line 25 - page 3, line 2. Since transfer gates 64 are "a type of bus switch" for controlling access to memory elements 62, and thus not capable of absorbing signals propagating down a data line stub, they do not disclose the recited bus line termination circuit. Klein, col. 5, ll. 59-61. Klein, therefore, does not anticipate claim 12, or claims 1, 25, or 29, and their corresponding dependent claims.

Claim 1 further recites *termination control logic to set the state of the termination circuitry according to decoded commands received on the address/command bus.* Claim 12 recites a similar limitation. The Examiner alleges Klein's state decoder 78 discloses the recited termination control logic. State decoder 78, however, does not disclose setting the state of *termination circuitry.* Klein, therefore, does not anticipate claim 1, or claim 12, and their corresponding dependent claims.

Claim 29 recites *transferring a register value to a termination parameter register in a memory unit served by a data bus, the register value including fields to indicate, to the memory unit, state conditions under which the memory unit should enable and/or disable a data bus line termination circuit on the memory unit.*

It appears the Examiner alleges Klein's control signals 68 disclose the recited register value. Control signals 68, such as "row address strobe (RAS), column address strobe (CAS) and write enable (WE) familiar to those in the art," however, do not include the recited fields, each field comprising at least one bit. See, Specification, page 9, line 12 – page 10, line 1; Klein, col. 5, ll. 52-55. Since Klein's control signals 68 do not include the recited fields, they

do not disclose the recited register value. Klein, therefore, does not anticipate claim 29 or its corresponding dependent claims.

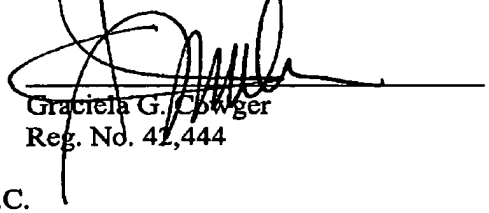
CONCLUSION

For the foregoing reasons, the Applicants request reconsideration and allowance of all claims as amended. The Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 32231

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613